

## **Perturbation of Copper Substitutional Defect Concentrations in CdS/CdTe Heterojunction Solar Cell Devices**

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### **ABSTRACT**

The efficacy of implementing terrestrial-based photovoltaics is dictated by trade-offs in device performance, cost, and reliability. Presently, the highest efficiency polycrystalline CdS/CdTe superstrate solar cells utilize back contacts containing copper as an intentional dopant. Accelerated stress data correlates copper diffusion from this contact with performance degradation. Degradation at the device level exhibits two characteristic modes that are influenced by CdTe surface treatments prior to contacting. Rapid degradation associated with a rapidly decreasing open-circuit voltage can occur in cases where processing favors stoichiometric CdTe surfaces. Slower degradation associated with roll-over is typified by treatments favoring the presence of Te at the back contact. The chemical composition and extent of Te-rich contact interfaces is revealed by transmission electron microscopy. Deep-level transient spectroscopy of NP etched and non-etched devices show Te-rich conditions are necessary for the detection of deep-acceptor  $\text{Cu}_{\text{Cd}}$  defect levels at ( $E_v + 0.28$  to  $0.34$  eV). Low keV cathodoluminescence measurements show that these defects can be found localized at the back surface of CdS/CdTe devices.

### **INTRODUCTION**

Owing to its nearly ideal bandgap, high absorption coefficient, and ease of film fabrication, polycrystalline CdTe is a promising candidate for low-cost, thin-film solar cells. Small-area CdS/CdTe cells with efficiencies of 15%-16% have been made by several research groups [1,2,3]. All use a standard device structure consisting of CdS/CdTe layers deposited on a transparent-conductor coated glass substrate. All structures also achieve high performance by utilizing a carbon or graphite-dag paste contact applied as a back contact to the top CdTe layer. In many (if not all) of these cases, Cu-containing dopants are mixed with the carbon layer to improve the ohmic nature of the contact. The exact mechanism by which this is achieved is somewhat unclear though several theories exist: 1) improved tunneling due to increased doping, 2) better band alignment due to fermi level adjustment, and 3) the formation of interfacial telluride layers [4].

Though beneficial to the initial device performance, Cu dopants introduce long-term device stability issues as measured through elevated temperature under illumination stress testing. A comparison of graphite-dag-based back contacts, with and without Cu constituents, substantiates this [5]. Finally, it has also been shown that precontact surface treatments (nitric-phosphoric acid and Br in MeOH) impact both the initial device performance and the relative stability of the contact [6]. In particular, it was the presence of elemental Te at the CdTe/back contact interface that determined the ultimate stability of the device.

## EXPERIMENTAL DETAILS

The polycrystalline CdTe/CdS films used in this study were deposited by close-spaced sublimation (CSS) and chemical bath deposition (CBD), respectively. These layers were grown on tin-oxide-coated Corning 7059 glass substrates. The respective CdTe and CdS layer thicknesses were  $\sim 8\text{ }\mu\text{m}$  and 80 nm. All devices utilized a  $400^\circ\text{C}$  anneal in vapor  $\text{CdCl}_2$  prior to the back contact process. Three precontact procedures were used: 1) no etching prior to contacting, 2) dilute ( $< 0.10\text{ vol}\%$ ) Br in MeOH etches, and 3) 1:88:35  $\text{HNO}_3\text{:H}_2\text{PO}_4\text{:H}_2\text{O}$  acid etches. These etches result in progressively more elemental Te being present on the CdTe surface prior to paste application.

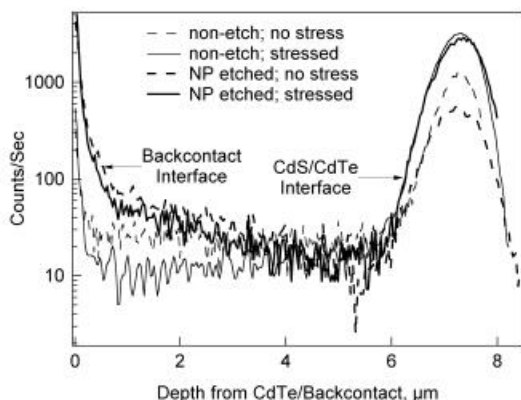
Pastes typically consist of mixing  $< 200$  mesh powders of  $\text{Cu}_{1.4}\text{Te}$  (Cerac) and HgTe in Cu:Hg proportions of between 5-10 at.%, with approximately four times that weight of graphite dag (Acheson Electrodag 114). After subsequent curing and dilution with methylethylketone (MEK), pastes are then applied by brushing to the CdTe surface. A subsequent  $260^\circ\text{C}$  anneal in helium activates the contact.

Compositional depth profiling measurements were performed using both x-ray photoelectron (XPS) and secondary ion mass (SIMS) spectroscopy. Where indicated, x-ray diffraction was performed using grazing-incidence (GIXRD) angles at or below the critical angle ( $\sim 0.3$  degrees) to distinguish between surface and bulk structure. Transmission electron microscopy (TEM) and energy dispersive x-ray spectroscopy (EDS) data were performed at 300 kV. Deep-level transient spectroscopy (DLTS) and low-voltage, scanning cathodoluminescence (CL) at 10 keV provided information regarding bulk and surface defect formation, respectively. Where necessary, dag-based back contacts are removed prior to analysis by ultrasonic stripping using MEK.

## DISCUSSION

The primary difference between samples discussed here is the amount of Te present between the CdTe and the Cu-containing dag back contact. The near-stoichiometric CdTe surface becomes increasing Te-rich as the Br:MeOH and NP etches are applied. Br:MeOH etches produce about 1-2 nm of Te, whereas NP etches produce hundreds of nm of Te as measured by XPS and confirmed by GIXRD.

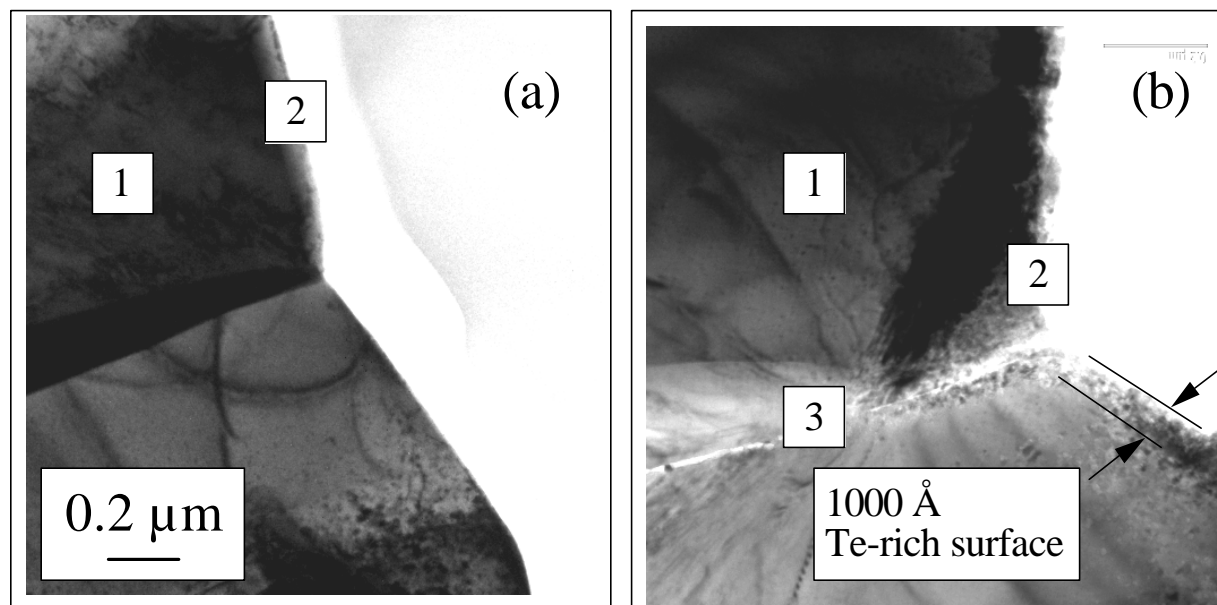
The distribution of Cu in unstressed and stressed devices, as a function of the amount of Te present measured by SIMS depth profiles for both NP-etched and non-etched films, is shown in figure 1.



**Figure 1.** Cu profiles in stressed and non-stressed CdTe/CdS polycrystalline devices for both NP-etched and non-etched back contact processes.

The SIMS data display several key features. In general, stress is shown to increase the amount of Cu present at the CdTe/CdS interface. When no stress is applied, NP-etched cells show the least amount of Cu at the interface. After stress, differences in Cu present at the heterojunction are not distinguishable in etched and non-etched devices. Cu is also seen to segregate at the backcontact interface more for NP-etched devices than non-etched devices. Also, the amount of Cu present at the back does not appear to vary significantly with stress. Finally, there is a subtle difference in the gradient of Cu measured as a function of distance away from the back contact interface for NP-etched and non-etched devices. The reason for this latter observation is possibly associated with how Te distributes itself during the NP etch process.

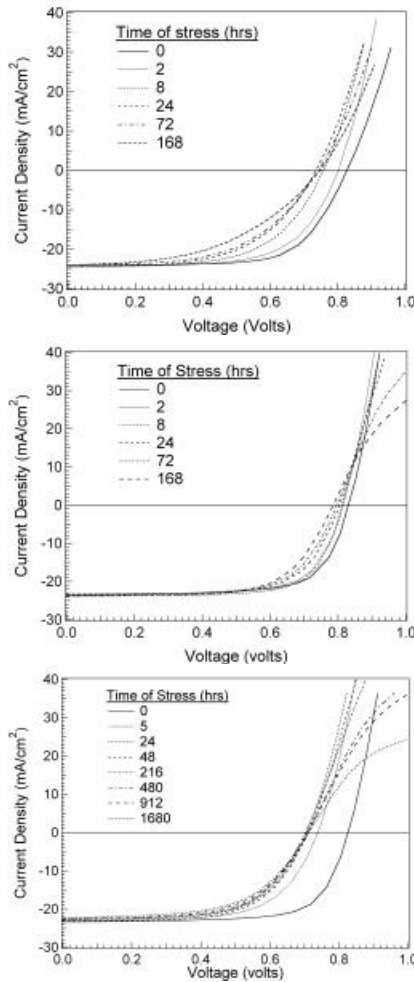
TEM images of non-etched and NP-etched devices (after back contact stripping) are shown in figure 2.



**Figure 2.** Bright-field TEM images of the CdTe/back contact interface after back contact stripping for (a) non-etched, and (b) NP etched back contacts.

In the absence of etching, CdTe grain boundaries are tightly compacted. Etching causes an obvious opening up of the grain boundary. We have measured such penetration at the grain boundary on the order of 1-2  $\mu\text{m}$ . EDX measurements were performed at the points indicated by numbers in figure 2. The corresponding Cd/Te peak (i.e., uncalibrated) ratios for points 1 and 2 in figure 2(a) were 2.1 and 2.0, respectively, suggesting a slight excess of Te at the surface of non-etched CdTe. After etching, the ratios for points 1, 2, and 3 in figure 2(b) were measured as 2.0, 0.5, and 1.1, respectively. The NP etch greatly increased the amount of Te at the CdTe surface relative to the bulk. This removal of Cd also results in a structurally modified surface layer approximately 100 nm thick, as shown in the figure 2. Free Te is also present at the grain boundary, and decreases in magnitude into the bulk of the CdTe. This decrease in Te down the grain boundary is mirrored by the gradient in Cu shown for the etched devices in figure 1. This suggests a close segregation of Cu with free Te in the CdTe layer. However, preliminary EDX measurements for Cu and/or  $\text{Cu}_x\text{Te}$  phases in Figure 2 do not substantiate this segregation effect. Rather, Cu is observed to permeate the sample area analyzed [7].

Device current-voltage measurements (I-V) of these cells as a function of accelerated stress testing (open-circuit bias, approximately 100°C, 1.5-2 suns illumination) are shown in figure 3.



*Case (a) No etching of CdTe/CdS structure prior to back contact application.*

*Case (b) NP etching of CdTe/CdS structure prior to backcontact application.*

*Case (c) Br:MeOH etch of CdTe/CdS structure prior to backcontact application.*

Figure 3. Variation in stress-induced IV degradation of CdTe/CdS devices utilizing different precontact surface treatments prior to back contact application.

Case (a) demonstrates a degradation mode that is rapid (within hours of stress) and characterized by a strong decrease primarily in open-circuit voltage ( $V_{oc}$ ). This mode is indicative of rapid diffusion of Cu to the interface, which has been shown will lower  $V_{oc}$  [8]. Case (b) shows another type of degradation. In this case, degradation is slower and occurs primarily through the introduction of increased roll-over in the 1<sup>st</sup> quadrant and a corresponding decrease in 4<sup>th</sup> quadrant fill factor. This type of degradation requires days to initiate and is back contact related [9]. An important feature of this degradation mode is that device performance can actually improve during the initial stages of stress, as shown by us previously [6]. Finally, case (c) demonstrates a combination of both types of degradation. First, there is the initial and rapid  $V_{oc}$  drop associated with case (a) occurring within the first few hours, followed by the roll-over characteristic of case (b) degradation after several days.

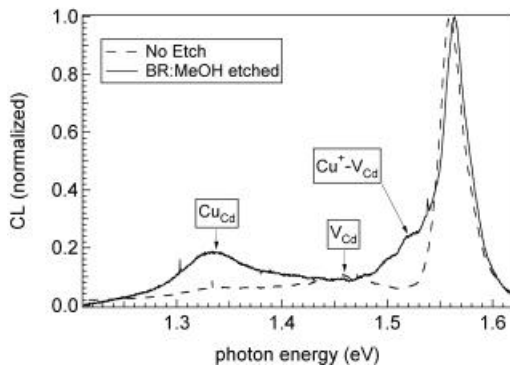
DLTS measurements were used to probe defect levels *near* the CdTe/CdS interface and *into the bulk* of the CdTe cell by increased reverse bias during measurement. The results for a series of stressed and unstressed cells with and without NP etching are shown in Table 1.

**Table 1.** DLTS electron (E1) and hole (H0, H1) hole trap energies and concentrations for NP-etched and non-etched CdTe/CdS devices with and without stress.

Stressed	Etch	E <sub>1</sub> (0.36 eV)	H <sub>0</sub> (0.28 eV)	H <sub>1</sub> (0.34 eV)
No	NP etched	$2.69 \times 10^{12}$	-	$8.1 \times 10^{12}$
No	NP etched	$8.3 \times 10^{11}$	-	$4.43 \times 10^{11}$
Yes	NP etched	$4.62 \times 10^{12}$	$5.7 \times 10^{11}$	$4.92 \times 10^{12}$
Yes	NP etched	-	$1.52 \times 10^{11}$	$5.53 \times 10^{11}$
No	No etch	$1.3 \times 10^{12}$	-	-
No	No etch	$6.55 \times 10^{11}$	-	-
Yes	No etch	-	-	-
Yes	No etch	$1.0 \times 10^{12}$	-	-

The E<sub>1</sub>, H<sub>0</sub>, and H<sub>1</sub> electron and hole traps are believed to be associated with Cu<sub>i</sub> and Cu<sub>Cd</sub> defects [10]. Although changes associated with stress were not discernible, it does appear that NP etches are necessary in order to see Cu<sub>Cd</sub> substitutional defects. This is not surprising because Te-rich environments should promote this type of defect.

These same latter defects were also observed at the back contact region by performing 10 keV CL measurements from that surface. At this voltage, penetration is approximately 0.5 μm into the CdTe. A comparison of Br:MeOH-treated and non-etched CdTe back contact surfaces is seen in figure 4.



**Figure 4.** Cathodoluminescence spectrum of non-etched and Br:MeOH-etched surfaces after removal of Cu-dag back contacts (non-stressed devices).

In non-Cu-doped CdTe films, there is usually a broad band of donor-to-acceptor pair (DAP) transitions associated with cadmium vacancies between 1.3 and 1.5 eV. This band is absent in figure 4 for the Br:MeOH-etched case, and greatly attenuated for the non-etched case. The absence or lessening of the DAP transition is caused by the quenching of these states by the incorporation of Cu into Cd vacancies and the formation of Cu<sub>i</sub><sup>+</sup>-V<sub>Cd</sub> complexes [11]. It is again obvious that etching favors the formation of these latter defects.

## CONCLUSIONS

Two separate and distinguishable degradation modes have been identified. One mode involves a rapid decrease in V<sub>oc</sub> with little introduction of 1<sup>st</sup> quadrant roll-over. The second

mode appears to be slower and is characterized by initial improvements in performance and subsequently, increased roll-over and decreased fill factor in the 1<sup>st</sup> and 4<sup>th</sup> quadrants, respectively. The first mode is associated with rapid diffusion of Cu<sup>+</sup> to the interface via bulk and grain boundary diffusion. When Te is present, the amount of mobile Cu<sup>+</sup> is reduced either through gettering effects associated with free Te at grain surfaces, or through the formation of shallow Cu<sub>i</sub><sup>+</sup>-V<sub>Cd</sub> complexes and/or deeper Cu<sub>Cd</sub> states. Thus, Te is seen as a way to initially moderate the rapid diffusion of Cu<sup>+</sup> to the interface. With longer stress times, increased roll-over suggests a redistribution in the Cu site occupancy at the back. One such mechanism would involve increased levels of the mobile Cu<sup>+</sup> species or deeper Cu<sub>Cd</sub> state at the expense of the more favored and shallower Cu<sub>i</sub><sup>+</sup>-V<sub>Cd</sub> states. Such a mechanistic shift would explain observed behaviors in I-V degradation.

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## REFERENCES

1. X. Wu, R. Ribelin, R. Dhere, D. Albin, T. Gessert, S. Asher, D. Levi, A. Mason, H. Moutinho, and P. Sheldon, Proceedings of the 28<sup>th</sup> IEEE Photovoltaic Specialists Conference, IEEE, New York, 470 (2000).
2. J. Britt and C. Ferekides, Appl. Phys. Lett. 62(22) 2851 (1993).
3. H. Ohyama, T. Aramoto, S. Kumazawa, H. Higuchi, T. Arita, S. Shibutani, T. Nishio, J. Nakajima, M. Tsuji, A. Hanafusa, T. Hibino, K. Omura, and M. Murozono, Proceedings of the 26<sup>th</sup> IEEE Photovoltaic Specialists Conference, IEEE, New York, 343 (1997).
4. B. E. McCandless, J.E. Phillips, and J. Titus, Proceedings of the 2<sup>nd</sup> World Conference and Exhibition on Photovoltaic Solar Energy Conversion, Vienna, Austria, 448 (1998).
5. J. Hiltner and J. Sites, in Proceedings of the 15<sup>th</sup> NCPV Photovoltaics Program Review Conference Proceedings, eds. M. Al-Jassim, J.P. Thornton, J.M. Gee, AIP Press, Vol 462, 170 (1998).
6. D. Albin, D. Levi, S. Asher, A. Balcioglu, R. Dhere, and J. Hiltner, Proceedings of the 28<sup>th</sup> IEEE Photovoltaic Specialists Conference, IEEE, New York, 583 (2000).
7. K. Jones, private communication.
8. K.J. Price, D. Grecu, D. Shvydka, and A.D. Compaan, Proceedings of the 28<sup>th</sup> IEEE Photovoltaic Specialists Conference, IEEE, New York, 658 (2000).
9. G. Stollwerck and J. Sites, Proceedings of the 13<sup>th</sup> European Photovoltaic Solar Energy Conference, 2020 (1995).
10. A. Balcioglu, R.K. Ahrenkiel, and F. Hasoon, J. of Appl. Phys., (88)12, 7175 (2000).
11. D. Grecu, A.D. Compaan, D. Young, U. Jayamaha, and D.H. Rose, J. of Appl. Phys., (88) 5, 2490 (2000).